

CLAIMS

What is claimed is:

- 1 1. A system for controlling peripheral devices in a computer system,
2 the system for controlling peripheral devices comprising:
3 a microcontroller that provides a plurality of device interfaces, each of the
4 device interfaces being adapted to support a peripheral device, and a
5 communication interface that is adapted to allow communication
6 between the communication interface and the peripheral devices;
7 and
8 a device that stores programming instructions to initialize the
9 microcontroller separately from the initialization of the computer
10 system.

- 1 2. The system set forth in claim 1, comprising an auxiliary power
2 source that supplies power to the microcontroller separately from a main power
3 supply that supplies power to the system.

- 1 3. The system set forth in claim 1, wherein the communication
2 interface comprises a Peripheral Component Interface ("PCI") interface.

1 4. The system set forth in claim 1, wherein the communication
2 interface comprises an Extended Peripheral Component Interface ("PCI-X")
3 interface.

1 5. The system set forth in claim 1, wherein the microcontroller
2 comprises a Streamlined Advanced Programmable Interrupt Controller ("SAPIC")
3 interface.

1 6. The system set forth in claim 1, wherein the microcontroller is
2 adapted to provide power management functionality for at least one of the
3 peripheral devices.

1 7. The system set forth in claim 1, wherein at least one of the
2 peripheral devices is a Super I/O controller.

1 8. The system set forth in claim 1, wherein the microcontroller is
2 defined to be a subtractive decode agent for the computer system.

1 9. The system set forth in claim 1, comprising reset logic that resets
2 the system under control of the microcontroller.

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2 10. The system set forth in claim 1, wherein the microcontroller
3 provides emulation for at least one of the peripheral devices.

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2 11. The system set forth in claim 1, comprising a local memory
3 associated with the microcontroller.

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2 12. A computer system, comprising:
3 a main power supply that provides power to the computer system;
4 a processor complex;
5 a system memory;
6 a memory controller that is connected to the processor complex and the
7 system memory to retrieve data from the system memory for the
8 processor complex;
9 a microcontroller that is connected to the memory controller, the
10 microcontroller providing a plurality of device interfaces, each of
11 the device interfaces being adapted to support a peripheral device,
12 and a communication interface that is adapted to allow
13 communication with the peripheral devices via the plurality of
14 device interfaces; and
15 a device that stores programming instructions to initialize the
16 microcontroller separately from the initialization of the computer
system.

1 13. The computer system set forth in claim 12, comprising an auxiliary
2 power source to supply power to the microcontroller.

1 14. The computer system set forth in claim 12, wherein the
2 communication interface comprises a Peripheral Component Interface (“PCI”)
3 interface.

1 15. The computer system set forth in claim 12, wherein the
2 communication interface comprises an Extended Peripheral Component Interface
3 (“PCI-X”) interface.

1 16. The computer system set forth in claim 12, wherein the
2 microcontroller comprises a Streamlined Advanced Programmable Interrupt
3 Controller (“SAPIC”) interface.

1 17. The computer system set forth in claim 12, wherein the
2 microcontroller is adapted to provide power management functionality for at least
3 one of the peripheral devices.

1 18. The computer system set forth in claim 12, wherein at least one of
2 the peripheral devices is a Super I/O controller.

1 19. The computer system set forth in claim 12, wherein the
2 microcontroller is defined to be a subtractive decode agent for the computer
3 system.

1 20. The computer system set forth in claim 12, comprising reset logic
2 that resets the system under control of the microcontroller.

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2 21. The computer system set forth in claim 12, wherein the
3 microcontroller provides emulation for at least one of the peripheral devices.

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2 22. The computer system set forth in claim 12, comprising a local
3 memory associated with the microcontroller.

1 23. A method of controlling peripheral devices in a computer system,
2 the method comprising the acts of:
3 initializing a microcontroller that includes a plurality of device interfaces,
4 each of the device interfaces being adapted to support a peripheral
5 device, the microcontroller comprising a communication interface

6 that is adapted to allow communication between the communication
7 interface and the peripheral devices; and
8 programming the microcontroller separately from the computer system.

1 24. The method set forth in claim 23, comprising the act of providing
2 auxiliary power to the microcontroller.

1 25. The method set forth in claim 23, comprising the act of defining a
2 Streamlined Advanced Programmable Interrupt Controller ("SAPIC") interface for
3 the microcontroller.

1 26. The method set forth in claim 23, comprising the act of employing
2 the microcontroller to provide power management functionality for at least one of
3 the peripheral devices.

1 27. The method set forth in claim 23, comprising the act of employing
2 the microcontroller to communicate with a Super I/O controller via at least one of
3 the device interfaces.

1 28. The method set forth in claim 23, comprising the act of defining the
2 microcontroller to be a subtractive decode agent for the computer system.

1 29. The method set forth in claim 23, comprising resetting the system
2 under control of the microcontroller.

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2 30. The method set forth in claim 23, comprising emulating at least one
3 of the peripheral devices.

1 31. A system for controlling peripheral devices in a computer system,
2 the system for controlling peripheral devices comprising:
3 means for interfacing with a plurality of peripheral devices via a
4 communication interface; and
5 a device that stores programming instructions to initialize the means for
6 interfacing separately from the initialization of the computer
7 system.

1 32. The system set forth in claim 31, comprising an auxiliary power
2 source that supplies power to the means for interfacing.

1 33. The system set forth in claim 31, wherein the communication
2 interface comprises a Peripheral Component Interface ("PCI") interface.

1 34. The system set forth in claim 31, wherein the communication
2 interface comprises an Extended Peripheral Component Interface ("PCI-X")
3 interface.

1 35. The system set forth in claim 31, wherein the means for interfacing
2 comprises a Streamlined Advanced Programmable Interrupt Controller ("SAPIC")
3 interface.

1 36. The system set forth in claim 31, wherein the means for interfacing
2 provides power management functionality for at least one of the peripheral
3 devices.

1 37. The system set forth in claim 31, wherein at least one of the
2 peripheral devices is a Super I/O controller.

1 38. The system set forth in claim 31, wherein the means for interfacing
2 is defined to be a subtractive decode agent for the computer system.

1 39. The system set forth in claim 31, comprising reset logic that resets
2 the system under control of the means for interfacing with a plurality of peripheral
3 devices.

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2 40. The system set forth in claim 31, wherein the means for interfacing
3 with a plurality of peripheral devices provides emulation for at least one of the
4 peripheral devices.

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2 41. The system set forth in claim 31, comprising a local memory
3 associated with the means for interfacing with a plurality of peripheral devices.

1 42. A computer system that comprises a microcontroller that functions
2 as a south bridge, the microcontroller being programmed to avoid conflicts with
3 other devices and to reduce resource consumption.